## Amendments to the Claims:

Please cancel claim 14 and amend claims 1, 4-7 and 9-12 as follows. The following listing of claims will replace all prior versions, and listings, of claims in the application:

## Listing of Claims:

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Claim 1 (Currently Amended). A sample assembly for a thermoelectric analyzer comprising:

- (a) an electrically-insulating substrate <a href="having a">having a</a>
  <a href="longitudinally-central region and two longitudinally-end regions">longitudinally-end regions</a>;
- (b) an adhesive layer disposed on said longitudinallycentral region and made of a material selected from a group
  consisting of indium and gold-tin alloy a pair of junction
  electrode layers non-contiguously formed on said substrate;
- (c) a pair of junction electrode layers formed on said two longitudinally-end regions respectively with certain distances from an adhesive layer disposed on said substrate, said adhesive layer being non-contiguous with said pair of junction electrode layers;
- (d) a sample fixed to said adhesive layer, said sample and
  15 being non-contiguous with said pair of junction electrode layers

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for thermostatic analysis in which an electric property of said sample is measured as a temperature of said sample varies;

- (e) a pair of electrode layers formed on <u>a top surface of</u> said sample; <del>and</del>
- 20 (f) two electrically-conductive wires, a first electricallyconductive wire connecting one of said electrode layers with one
  of said junction electrode layers, and
  - (g) a second electrically-conductive wire connecting the other of said electrode layers with the other of said junction electrode layers wherein an electrical property of the sample is measured as a temperature of the sample varies.

Claim 2 (Original). A sample assembly according to claim 1, wherein said adhesive layer is made of indium.

Claim 3 (Original). A sample assembly according to claim 2, wherein said substrate is made of a material selected from a group consisting of aluminum nitride, boron nitride, beryllium oxide and aluminum oxide.

Claim 4 (Currently Amended). A sample assembly according to claim 3, wherein each of said pair of electrode layers and said

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pair of junction electrode layers is made of a multilayer
including a top layer which is a gold layer, and said <u>first and</u>
second electrically-conductive wires are gold wires.

Claim 5 (Currently Amended). A sample assembly according to claim 4, wherein said pair of electrode layers, said pair of junction electrode layers and said <u>first and second electrically-conductive</u> wire means wires are arranged mirror-symmetrical with respect to a center of said sample.

Claim 6 (Currently Amended). A sample assembly according to claim 5, wherein said sample is <u>a</u> compound semiconductor.

Claim 7 (Currently Amended). A sample assembly according to claim 1, wherein said adhesive layer is made of a gold-tin alloy.

Claim 8 (Original). A sample assembly according to claim 1, wherein said substrate is made of a material selected from a group consisting of aluminum nitride, boron nitride, beryllium oxide and aluminum oxide.

Claim 9 (Currently Amended). A sample assembly according to claim 1, wherein said sample assembly is adapted to be supported

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by two support rods which <u>also</u> serve <del>also</del> as conductors for an electric circuit, and <u>wherein</u> gold washers are inserted between said support rods and said junction electrode layers.

Claim 10 (Currently Amended). A sample assembly according to claim 1, wherein each of said electrode layers and said junction electrode layers is made of a multilayer including a top layer which is a gold layer, and said <u>first and second</u> electrically-conductive wire means wires are gold wires.

Claim 11 (Currently Amended). A sample assembly according to claim 1, wherein said pair of electrode layers, said pair of junction electrode layers and said <u>first and second electrically-conductive wires</u> wire means are arranged mirror-symmetrical with respect to a center of said sample.

Claim 12 (Currently Amended). A sample assembly according to claim 1, wherein said sample is  $\underline{a}$  compound semiconductor.

Claim 13 (Original). A sample assembly according to claim 1, wherein said sample has a plane size of 5 mm  $\times$  5 mm or less.

Claim 14 (Cancelled).

## Amendments to the Drawings:

The attached sheets of drawings include changes to Fig. 5. Specifically, attached hereto is an annotated sheet showing changes to Fig. 5 and a replacement sheet for Fig. 5 which includes the changes thereto. The changes to Fig. 5 are directed to a portion which was previously not translated from Japanese into English at the time the present application was filed. The amendment of Fig. 5 is supported by the application as originally filed (see page 15, lines 17-21 of the present application).

Attachments: Marked sheet showing changes to Fig. 5

Replacement sheet for Fig. 5